Phase-Locked Loops (PLL)


**Introduction**

- The phase-locked loop concept was first developed in the 1930s. It has since been used in communications systems of many types, particularly in satellite communications systems.
- Until recently, however, phase-locked systems have been too complex and costly for use in most consumer and industrial systems, where performance requirements are more modest and other approaches are more economical.
- The PLL is particularly amenable to monolithic construction, however, and integrated-circuit phase-locked loops can now be fabricated at very low cost.
- Their use has become attractive for many applications such as FM demodulators, stereo demodulators, tone detectors, frequency synthesizers, and others.

**Definition**

- A PLL is a feedback system that includes a Voltage-Controlled Oscillator (VCO), phase detector, and low pass filter within its loop.
- Its purpose is to force the VCO to replicate and track the frequency and phase at the input when in lock.
- The PLL is a control system allowing one oscillator to track with another.
- It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track.

\[
\omega_{\text{out}}(t) = \omega_{\text{in}}(t)
\]

\[
\phi_{\text{out}}(t) = \phi_{\text{in}}(t) + \text{const.}
\]

**Notes**

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Depending on the application, the PLL output can be taken from either:

1. $V_{cont}$, the filtered (almost DC) VCO control voltage,
2. or from the output of the VCO

- The former provides a baseband output that tracks the phase variation at the input.
- The VCO output can be used as a local oscillator or to generate a clock signal for a digital system.
- Either phase or frequency can be used as the input or output variables.
- Of course, phase and frequency are interrelated by:

$$\omega(t) = \frac{d\phi}{dt} \quad \text{and} \quad \phi(t) = \phi(0) + \int_0^t \omega(t') dt'$$

Applications:

- There are many applications for the PLL:
  1. FM demodulator
  2. Frequency synthesizer
  3. Clock generation

- You should note that there will be different input and output variables and different design criteria for each case,
- but you can still use the same basic loop topology and analysis methods.
Phase detector:

- **Phase detector** compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs.
- $K_p$ is the gain of the phase detector (V/rad).

\[ v_e(t) = K_p \left( \phi_1(t) - \phi_2(t) \right) \]

- As one familiar circuit example, an analogue multiplier (Gilbert cell) can be used as a phase detector.
- Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$.

\[
A(t)B(t) = AB \cos(\omega_d t + \phi_d) \cos(\omega_r t + \phi_r) = \\
\left( \frac{AB}{2} \right) \left[ \cos(2\omega_d t + \phi_d + \phi_r) + \cos(\phi_d - \phi_r) \right]
\]

Since the two inputs are at the same frequency when the loop is locked, we have:

1. one output at twice the input frequency and
2. an output proportional to the cosine of the phase difference.

The doubled frequency component must be removed by the lowpass loop filter.

Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.
The averaged transfer characteristic of such a phase detector is shown below.

- Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).
- If the phase difference is $\pi/2$, then the average or integrated output from the XOR-type phase detector will be zero (or $V_{DD}/2$ for single supply, digital XOR).
- The slope of the characteristic in either case is $K_D$.

In PLL applications, the VCO is treated as a linear, time-invariant system.

- Excess phase of the VCO is the system output.
- The VCO oscillates at an angular frequency, $\omega_{out}$. Its frequency is set to a nominal $\omega_0$ when the control voltage is zero.
- Frequency is assumed to be linearly proportional to the control voltage with a gain coefficient $K_O$ or $K_{VCO}$ (rad/s/v).
- Thus, to obtain an arbitrary output frequency (within the VCO tuning range), a finite $V_{cont}$ is required.
- Let’s define $\phi_{out} - \phi_{in} = \Delta \phi$.

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In the figure below, the two inputs to the phase detector are depicted as square waves.

The XOR function produces an output pulse whenever there is a phase misalignment.

Suppose that an output frequency $\omega_1$ is needed. From the upper right figure, we see that a control voltage $V_1$ will be necessary to produce this output frequency.

The phase detector can produce this $V_i$ only by maintaining a phase offset $\phi_0$ at its input.

In order to minimize the required phase offset or error, the PLL loop gain, $K_DK_{p0}$, should be maximized, since

$$\phi_0 = \frac{V_i}{K_D} = \frac{\omega_1 - \omega_0}{K_DK_{p0}}$$

Thus, a high loop gain is beneficial for reducing phase errors.
To see how the PLL works, suppose that we introduce phase step at the input at \( t = t_1 \). So that,

\[
\phi_p = \omega_1 t + \phi_1 + \phi_0 (t - t_1)
\]

Since we have a step in phase, it is clear that the initial and final frequencies must be identical: \( \omega_2 \).

But, a temporary change in frequency is necessary to shift the phase by \( \phi_1 \).

The area under \( \omega_{out} \) gives the additional phase because \( V_{cont} \) is proportional to frequency.

\[
\phi_1 = \int \omega_{out} \, dt = \int K_d V_{cont}(t) \, dt
\]

After settling, all parameters are as before since the initial and final frequencies are the same.

This shows that \( V_{cont}(t) \) can be used to monitor the dynamic phase response of the PLL.
Dynamic Response ($\Delta \omega$)

- Now, let’s investigate the behaviour during a frequency step: $\omega_f = \omega_f + \Delta \omega$
- The will cause the phase difference to grow with time
- This in turn causes the control voltage, $V_{\text{cont}}$, to increase, moving the frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp.
- This in turn causes the $V_{\text{cont}}$ to increase, moving the VCO frequency up to catch up with the input reference signal.

In this case, we have a permanent change in $\omega_{\text{out}}$ since a higher $V_{\text{cont}}$ is required to sustain a higher $\omega_{\text{out}}$.

If the frequency step is too large, the PLL will lose lock.

PLL in Locked Condition

- **Approach:** We will discuss the details of phase detectors and loop filters as we proceed.
- But, at this point, we will treat the PLL as a linear feedback system.
- We assume that it is already “locked” to the reference signal, and examine how the output varies with the loop transfer function and input.
- A frequency domain approach will be used, specifically describing transfer functions in the s-domain.
  
  $V_f(s)/\Delta \phi = K_D$ and $\phi_{\text{out}}(s)/V_{\text{cont}}(s) = K_{\text{CF}}s$

Note that the VCO performs an integration of the control voltage and thus provides a factor of $1/s$ in the loop transfer function.

Because of this, a PLL is always at least a first order feedback system.
PLL as Feedback System.

- **Loop Gain:**
  \[ T(s) = K_{PD}(s)K_{PD}(s) \]
  \[ T(s) = \frac{K_{PD}(s)}{1+T(s)} \]

- **Transfer Function:**
  \[ \frac{OUT(s)}{IN(s)} = H(s) = \frac{K_{PD}(s)}{1+T(s)} \]

- The Loop gain can be described as a polynomial:
  \[ T(s) = K'(s+a)(s+b) \cdots \frac{s}{s+a}(s+b) \cdots \]

- **ORDER** – the order of the polynomial in the denominator
- **TYPE** – n (the exponent of the s factor in the denominator)
- **PHASE ERROR**
  \[ \epsilon(s) = \frac{OUT(s)}{\left[1+T(s)\right]} \]

- **STEADY STATE ERROR**
  \[ \epsilon_{ss} = \lim_{t\to\infty} [\epsilon(s)] = \lim_{t\to\infty} \epsilon(t) \]

Notes

PLL as a first-order filter

The closed-loop gain transfer function is given by

\[ V_o \over \omega = K_{PD}F(s)A \over 1+K_{PD}F(s)A - (K_{OA} = s) \]

Assuming
\[ \omega = \frac{d\varphi}{dt} \text{ then } \omega = s\varphi(s) \]

The transfer function in terms of frequency variations therefore can be expressed as:

\[ V_o \over \omega = \frac{1}{\omega} V_o \over \omega = \frac{K_{PD}F(s)A}{s + K_{PD}F(s)A - K_{OA}} \]

Assuming that LP is removed and \( K_{PD}F(s)A \), hence

Thus the loop inherently produces a first order low-pass transfer characteristic

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PLL as a first-order filter

Assuming that LP is removed and \( K_v = K_0 A \), hence

Thus the loop inherently produces a first order low-pass transfer characteristic.

Example

A PLL has a \( K_0 \) of \( 2\pi /1 \text{kHz/V} \), a \( K_v \) of 500 s\(^{-1}\) and a free-running frequency of 500Hz. Find \( V_o \) for a constant input signal frequency of 250 Hz and 1 kHz

\[
V_o = \left( \omega_i - \omega_o \right) / K_v
\]

At 250 Hz,

\[
V_o = \left( 2\pi(250) - 2\pi(500) \right) / 2\pi(1 \text{kHz/V}) = -0.25V
\]

At 500 Hz

\[
V_o = \left( 2\pi(1000) - 2\pi(500) \right) / 2\pi(1 \text{kHz/V}) = 0.5V
\]
PLL as a first-order filter

- This example shows that PLL can operate with no loop filter
- Nevertheless it has several practical drawbacks.
- Since the phase detector is really a multiplier, it produces a sum frequency component at its output as well as the difference frequency component.
- This component at twice the carrier frequency will be fed directly to the output if there is no loop filter.
- Also, all the out-of-band interfering signals present at the input will appear, shifted in frequency, at the output.
- Thus, a loop filter is very desirable in applications where interfering signals are present.

Second-order PLL

- The most common configuration for integrated circuit PLLs is the second-order loop.
- Here, loop filter $F(s)$ is simply a single-pole, low-pass filter, usually realized with a single resistor and capacitor. Thus
- Substituting this into

$$F(s) = \frac{1}{1 + s/\omega_0}$$

- It gives:

$$V_o = \frac{1}{s} \frac{K_v F(s)}{s + K_v F(s) A K_v}$$

- The roots of this transfer function are

$$s_{1,2} = -\frac{\omega_0}{2} \left( 1 \pm \sqrt{1 - \frac{4K_v}{\omega_0}} \right)$$

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This transfer function can be also expressed as:

\[ V_o = \frac{1}{\omega_o} \frac{1}{s^2 + \frac{2\zeta}{\omega_o}s + 1} \]

\( \omega_o = \sqrt{\omega_1 K_v} \) is crossover frequency

\( \zeta = \frac{1}{2} \sqrt{\frac{K_v}{\omega_1}} \) is damping factor

We can have a very underdamped response when \( \omega_1 \ll K_v \).

Think about the inverse Laplace transform of the complex conjugate pole pair.

The inverse Laplace transform of the complex conjugate pole pair gives

\[ s_{1,2} = -\frac{\omega_1}{2} \left( 1 \pm \sqrt{1 - \frac{4K_v}{\omega_1}} \right) \]

A good compromise is using a maximally flat low-pass pole configuration in For this response, the damping factor should be equal to \( \frac{1}{\sqrt{2}} \).

Thus

\[ v(t) = e^{-\frac{\omega_1}{2}t} \sin \left( \frac{\omega_1}{2} \sqrt{1 - \frac{4K_v}{\omega_1}} t \right) \]

\[ \zeta = \frac{1}{2} \sqrt{\frac{K_v}{\omega_1}} = \frac{1}{\sqrt{2}} \text{ and } \omega_1 = 2K_v \]
PLL open-loop response with no loop filter

PLL open-loop response with a single-pole filter

The introduction of the first-order LP filter relieves an extra Zero at higher frequency in loop transfer function, the phase shift is now close to $-180^\circ$ and a system may become unstable.

PLL open-loop response with zero added in loop filter

Adding a resistor to the lowpass loop filter contributes a Zero to its transfer function

$$F(s) = \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

Thus, the zero frequency is always higher than the pole frequency, $\omega_z > \omega_p$.
**Lock Range**

- **Lock Range.** Range of input signal frequencies over which the loop remains locked once it has captured the input signal. This can be limited either by the
  - (a) phase detector or
  - (b) the VCO frequency range.
- If limited by phase detector: $0 < \varphi < \pi$ is the active range where lock can be maintained.

[Diagram of Lock Range]

For the phase detector type shown (Gilbert multiplier or mixer), the voltage vs. phase slope reverses outside this range. Thus the frequency would change in the opposite direction to that required to maintain the locked condition. The maximal voltage from the phase detector in active (locked) region is $V_{v_{\text{max}}} = \pm K_p \pi/2$

This voltage amplified by the gain $A$ is applied through the loop filter to the VCO and produces a frequency shift:

$$\Delta f_{\text{VCO}} = A \cdot K_p K_D (\pi/2) = K_v (\pi/2)$$

where $K_v = AK_p K_D$ is a loop gain gains.

If the input frequency is shifted away from the free-running value outside this range, the loop will lose lock, otherwise it stays lock.

Therefore the lock range is given by:

$$\omega_{\text{L}} = K_v (\pi/2)$$
This is the frequency range around the free running frequency that the loop can track.
- Doesn’t depend on the loop filter
- Does depend on DC loop gain
- The lock range could also be limited by the tuning range of the VCO limited by capacitance ratios or current ratios. In many cases, the VCO can set the maximum lock range.

Capture range:
- Range of input frequencies around the VCO centre frequency onto which the loop will lock when starting from an unlocked condition and is always less than the lock range.
- When the input frequency is swept through a range around the center frequency, the output voltage as a function of input frequency displays a hysteresis effect.
Assume that the loop is opened at the loop-amplifier output and that a signal with a frequency not equal to the free-running VCO frequency is applied at the input of the PLL.

The sinusoidal difference frequency component that appears at the output of the phase detector has the value

\[ V_{pd}(t) = \frac{\pi}{2} K_o \cos(\omega_d - \omega_{vco}) \]

Capture Range

The output from the loop amplifier thus consists of a sinusoid at the difference frequency whose amplitude is reduced by the loop filter.

This component is passed through the loop filter, and the output from the loop amplifier resulting from this component is

\[ V_o(t) = \frac{\pi}{2} K_o A \cdot |F(j(\omega_d - \omega_{vco}))| \cos(\omega_d - \omega_{vco}) \]

In order for capture to occur, the magnitude of the voltage that must be applied to the VCO input is

\[ V_{vco}(t) = \frac{\omega_o - \omega_{vco}}{K_o} \]

Capture is likely to occur when \( V_{vco}(t) < V_o(t) \) Therefore:

\[ \omega_o = \omega_d - \omega_{vco} < \frac{\pi}{2} K_o A \cdot |F(j(\omega_d - \omega_{vco}))| \]

The Capture Range is always lower than the Lock Range

\[ \omega_o = \frac{\pi}{2} - K_o A |F(j(\omega_d - \omega_{vco}))| < \omega_L = \frac{\pi}{2} - K_f \]

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Typical Question

The 2nd-order phase-locked loop (PLL) system illustrated in Fig. 2 contains sub-elements with corresponding gain values as shown in Table 1. The amplifier gain may be assumed to be constant.

Table 1. Gains

<table>
<thead>
<tr>
<th>Component</th>
<th>Symbol</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase Detector</td>
<td>KD</td>
<td>50</td>
<td>volts/radian</td>
</tr>
<tr>
<td>VCO</td>
<td>KO</td>
<td>10^6</td>
<td>Radians/sec/volt</td>
</tr>
<tr>
<td>Amplifier</td>
<td>A</td>
<td>20</td>
<td>dB</td>
</tr>
</tbody>
</table>

Given loop-filter component values $R_1 = 5.6 \, k\Omega$, $R_2 = 330 \, \Omega$ and $C = 1 \, nF$, sketch

(a) the asymptotic closed-loop ($V_o/\omega_1$) PLL frequency response and estimate the bandwidth and

(b) the asymptotic loop-gain response and graphically or otherwise, determine the 0 dB intercept frequency

(c) Explain the advantages of using second–order low-pass filter in PLL system with a help of open-loop response.

Notes

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The transfer function of low-pass filter is:
\[ F(s) = \frac{1 + s/\omega_o}{1 + s/\omega_i} \]

where the pole:
\[ \omega_o = \frac{1}{(R_C + R_L)C} = \frac{10^3}{5600 + 330} = 1.7 \times 10^3 \text{rad/s} \]

and zero:
\[ \omega_i = \frac{1}{RC} = \frac{10^3}{150} = 3 \times 10^3 \text{rad/s} \]

The closed-loop PLL frequency response is:
\[ \frac{V_o}{V_i} = \frac{1 + s/\omega_o}{1 + s/\omega_i} \cdot \frac{K_i(F(s))}{s + K_i F(s) + (1 + K_o/\omega_i)} \]

The roots (poles) of:
\[ s^2/\omega_o + s(1 + K_i/\omega_o) + K_o = 0 \]

are:

\[ s = \frac{-1 + \sqrt{1 + 4K_o/\omega_o}}{2/\omega_o} \]

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The poles are:
\[ \omega_p_1 = \frac{-166 + 125}{1.19 \times 10^3} = -3.43 \times 10^3 \text{rad/s} \]
\[ \omega_p_2 = \frac{-166 - 125}{1.19 \times 10^3} = -2.46 \times 10^3 \text{rad/s} \]
Solution

The low frequencies gain ($\omega \rightarrow 0$) is $1/K_v = 10^{-6} = -120$ dB

Pole and Zero effectively cancel each other, therefore the bandwidth is $\omega_p = 2.46 \cdot 10^7$ rad/sec $\approx 4$ MHz

(b) The loop gain of PLL is

$$L(s) = \frac{K_v A F(s)}{s} = \frac{K_v}{s} \frac{1 + \frac{s}{\omega_p}}{1 + \frac{s}{\omega_s}}$$

With no loop filter the gain is which has 0 dB frequency at $K_v = 5 \times 10^9$ rad/s

For $-20$ dB slop $L_2 = \frac{\omega_p}{\omega_s}$ and therefore:

$$L_2 = \frac{L_2}{L_v} = \frac{5 \times 10^6}{1.7 \times 10^6} = 3 \times 10^3 \cdot 2 \times 10^{-2} = 9.6 = 19.6$ dB

And finally

$$\omega_s = \omega_0 \frac{L_2}{L_v} = 3 \times 10^7 \frac{9.6}{1} = 2.8 \times 10^7 \text{ rad/s}$$