Lecture 4.
Ramp and Signal Generation

Preface

In the first years of microelectronics, analog integrated circuits were mainly considered to perform calculations in the so-called analog computers.

Nowadays, analog computers are completely forgotten due to the digital rivals.

Moreover, a striking drop in price in digital technologies gives rise a new area: Digital Signal Processing (DSP).

Digital electronics has opened many new application areas for electronics.

This has increased the need for processing analog signals because our world is essentially analog and the signals coming from it are analog.

Syllabus II

Function Generation and Signal Transformation
- Voltage and current ramp generation techniques: IC and device-based approaches.
- Diode shaping circuits: functional approximation, sine-wave generation.
- Log and anti-log amplifier design: thermal and frequency stability; range considerations.
- Analog multipliers: design alternatives; the Gilbert-cell, prewarping; linear multiplier, modulator, phase-detector.
- Multiplier IC applications: AGC, division, function generation, level control.
- Voltage-controlled oscillator design.
- The phase-locked loop: components and operation; second-order loop analysis; applications.

Analog Signal Processing

This chapter deals with processing (continuous) instrumentation signals using integrated circuits (ICs) as well as discrete parts.

Analog signal processing circuits are present in most applications using sensors because most sensors yield analog signals.

The design of these circuits cannot be automated like that of some digital circuits.

Nevertheless a systematic approach to design is still possible by first considering the nature of the signals to be processed and the process to be performed.
Analog signal processing is faster than digital signal processing but it is less flexible.

Analog signal processing deals with:
- adapting the amplitude, bandwidth, and impedance of signals;
- converting signals from one analog domain to another;
- performing operations such as addition, comparison, and synchronous detection;
- analog-to-digital and digital-to-analog conversion;
- and minimizing interference and reducing noise, etc...

Here we consider two important area of ASP:
- signal generation
- signal transformation

In this part we consider:
- Linear Ramp / Triangle / Sawtooth
- Rectangular / Square / Pulse
- Exponential
- Sinusoidal
- Arbitrary / Non-Linear
- Controlled

Response Linearisation
Range Compression
Functional Inversion
Logarithmic / Anti-Logarithmic
Multiplication / Division
Modulation
Most Function Generators produce signal in three main waveforms: triangular, square-wave, and sinusoidal.

Here is the Generalized Form of a Function Generator:

- Control Unit
- External Signal
- Primary Signal Generator
- Transformation Module(s)
- Output(s)
- Feedback Module

Exam Question 1c (2000)

1 c) Outline an approach to the generation of triangular, square, and sinusoidal functions, which could be adopted by integrated circuit (IC) designers.

[5 marks]

Solution

- \( I_1 \) and \( I_2 \) are matched current sources.
Notes

Ramp approaches

1. Based on Current mirror (saw-tooth and triangular wave)
2. Bootstrap Approach (saw-tooth wave)
3. Integrator Approach (saw-tooth and triangular wave)
Current mirror (simple)

- The simplest form of current source is based on two BJTs.
- Q1 is diode connected forcing $V_{CB1}=0$. It behaves as forward biased diode B-E.
- Since Q1 and Q2 have the same $V_{EB}$, their collector current are equal: $I_{C1}=I_{C2}$.
- Summing currents on collector C1 yields:
  $$I_{ref}-I_{C1}-I_{B1}-I_{B2}=I_{ref}-I_{C1}-2I_{C1}/\beta_F=0$$
- Therefore:
  $$I_{C1} = I_{ref}/(1 + 2/\beta_F) = I_{C2}$$
- If $\beta_F$ is large the collector current of Q2 is nearly equal to reference current:
  $$I_{C2} \approx I_{ref} = \frac{V_{CC} - V_{BE1a}}{R}$$
- Since current current of Q2 is reflected in the output, this circuit is often called current mirror.

Charging Cycle

- At $V_{cont}=0$ V Q3 is closed as well as Q1 and Q3.
- A constant charging current $I$ flows through the D2 and produces a linear variation in capacitor voltage with time:
  $$V_c(t) = I \cdot t / C$$
Q3 is turned ON by the rising base signal: \( V_{e1} = V_{e2} = 0 \)
- The CCS current \( I \) flows in Q1 and is mirrored in Q2.
- The capacitor voltage falls at a rate of \( \frac{I \cdot t}{C} \).
Ramp Slope-Error

A circuit with an exponential response may be used to generate a linear voltage ramp over a small voltage range 0 - V and time T, but there will inevitably be some

- **slope-errors** = [initial slope - final slope]/[initial slope].
- In this case: $V_c(t) = V_f\left[1 - \exp(-t/RC)\right] = E\left[1 - \exp(-t/RC)\right]$
- The slope of the exponential at time $t$ is:
  \[ \frac{dV_c(t)}{dt} = \frac{E}{RC}\exp(-t/RC) \]
- Hence: $\varepsilon = \frac{E}{RC}\left[1 - \exp(-t/RC)\right]/\left[E/RC\right] = \left[1 - \exp(-t/RC)\right]$
- and finally $\varepsilon = V_c(t)/V_f = V/V_f = V/E$

A Bootstrap Ramp Generator

- Slope-error performance may be determined either from an analysis of $V_c$ or of $V_o$:
  \[ V_o(t) = GV_c(t) = \left(G/C\right)\int t(t)dt = \left(G/RC\right)\left[V_o(t) + E - V_c(t)\right]dt \]
Bootstrap Ramp Generator

But: \[ V_o(t) = \frac{V_o}{G} \]

Therefore: \[ V_o(t) = \left(\frac{G}{RC}\right) \left[ V_o(t)[1-1/G] + E \right] dt \]

Hence: \[ \frac{dV_o(t)}{dt} = \left(\frac{G}{RC}\right) \left[ V_o(t)[1-1/G] + E \right] \]

If \( V_o(0) = V_o(0) = 0 \) and the ramp is terminated when \( V_o = GV \), then

\[ e = \left(\frac{G}{RC}\right) E - GV[1-1/G] + E \left(\frac{EG}{RC}\right) = \frac{1}{E} \left[ -GV[1-1/G] \right] = V[1-G]/E \]

Hence, the slope error is zero for \( G = 1 \),

For linear ramp current charging capacitor must be constant:

\[ I_c(t) = \frac{E + V_o(t) - V_o(t)}{R} \]

Using: \( V_o(t) = G \cdot V_c(t) \)

Therefore the current is:

\[ I_c(t) = \frac{E + G \cdot V_c(t) - V_c(t)}{R} = \frac{E + (G-1) \cdot V_c(t)}{R} \]

Hence, for \( G = 1 \) the current \( I_c(t) \) is time-independent:

\[ I_c(t) = \frac{E}{R} \]

This circuit is non-practical due to the problems in creating floating (non-grounded) constant voltage source.
With ideal components, a linear ramp will only be produced if the charging current $I$ is maintained constant, i.e., if the voltage across $R$ is constant.

Just before the switch is opened: $V_2 = +E; V_D = V_I = 0$

When the switch opens, $V_r$ and $V_0 = GV$ start to rise and $D_1$ is immediately reverse biased - the constant voltage supply $E$ is hence isolated from the charging circuit.

During charging of $C_2$, the current $I$ is derived only from charge lost by $C_2$:

$$\Delta Q = C_1 \Delta V_1 = C_1 \Delta V_2; \quad \Delta V_1 = V_I$$

$$\Delta V_2 = \left(\frac{C_1}{C_2}\right) \Delta V_1 = V_I \left(\frac{C_1}{C_2}\right)$$
Design Analysis (cont.)

Charging current is hence:

\[ I = \frac{V_O + V_2 - V_1}{R} = \left[ \frac{(G-1)V_1 + V_2}{R} \right] \]

Substituting for \( V_2 \):

\[ V_2 = GV_1 = E - \Delta V_2 = E - V_1 \left( \frac{C_1}{C_2} \right) \]

\[ I = \left[ \frac{(G-1-C_1/C_2)V_1 + E}{R} \right] \]

For linear ramp (\( I = E/R \)) it is required that \( G = 1 + \left( \frac{C_1}{C_2} \right) \)

\[ G = 1 + \left( \frac{R_1}{R_2} \right) \]

\[ \frac{R_1}{R_2} = \frac{C_1}{C_2} \]

Bootstrap Ramp Generator (shortcut)

For linear ramp current charging capacitor must be constant

\[ I_c(t) = \frac{V_{c_2} + V_O(t) - V_{c_1}(t)}{R} \]

Using: \( V_O(t) = G \cdot V_{c_1}(t) \)

Therefore the current is:

\[ I_c(t) = \frac{E - \Delta V_{c_2} + GV_{c_1}(t) - \Delta V_{c_1}(t)}{R} \]

\[ \Delta Q = C_1 \cdot \Delta V_1 = C_2 \cdot \Delta V_2; \quad \Delta V_1 = V_1 \]

\[ I_c(t) = \frac{E - C_1/C_2 \cdot V_{c_1}(t) + GV_{c_1}(t) - V_{c_1}(t)}{R} = \frac{E + (G - C_1/C_2 - 1) \cdot V_{c_1}(t)}{R} \]

Hence, the current \( I_c(t) \) is time-independent if:

\[ G - C_1/C_2 = 1 = 0 \quad \text{or} \quad G = C_1/C_2 + 1 \]

For \( C_1 = C_2 \), the gain \( G = 2 \) and \( R_1 = R_2 \)
1. (a) Outline one method of generating a linearly changing current (ramp) in an inductor assuming that the inductor has an associated series (winding) resistance. [5 marks]

**SOLUTION**

- For linear current ramp \( I(t) = k \ t \). Then
  
  \[ V(t) = L \frac{di}{dt} + i \times r = kL + krt \]

- This represent ramp + pedestal waveform, which may be expressed as
  
  \[ kL = 2IR^2 = \frac{2E}{R} \]

- Finally
  
  \[ \frac{2I}{C} = kr = \frac{2E}{RC} \]
TTL Switching:
Capacitor Discharge

Discharge Mechanism

- Input voltage \( V_s \) at logic low (< 0.4V).
- B-E junction of \( Q_1 \) conducting but no collector current available – \( Q_2 \) is OFF.
- Input voltage \( V_s \) rises to logic high (>2.4V). B-E junction of \( Q_1 \) is reverse biased.
- B-C junction of \( Q_1 \) and B-E junction of \( Q_2 \) brought into conduction - \( I_B \) flows.
- Rapid input change may create a brief rise in \( V_1 \) due to inter-electrode capacitance feedthrough.
- \( I_{C2} = I_B + I \) rises rapidly to large constant value ( \( =bI_B \) ) – \( C_1 \) rapidly discharged after initial turn-on delay.
- While \( V_{CE2} = V_1 > 0.2V \) \( Q_2 \) operates in its active region and discharge is linear - saturation slows final fall.
TTL Switching: Ramp Initiation

+5V

Input voltage $V_s$ falls to $< 0.4V$ - Emitter current of $Q_1$, $I_{b1}$, flows.

$Q_2$ draws an initial collector current from charge stored in the base of $Q_2$ - a reverse base current $I_{b2}$

$I_{b2}$ is relatively large (mA) and depletes the base of $Q_2$, turning $Q_2$ OFF very quickly - $I_{c2}$ tails from current $I$ to 0.

The effect of this sudden switching often results in some charge being drawn out of $C_1$ - $V_1$ falls below 0V.

The initial start point of the ramp will be offset from 0V - the effect increases for small values of $C_r$.

The provision of a constant charging current $I$ causes $V_1$ to increase linearly.

Switch Turn-Off Mechanism

$V_s$
Design Problem A

- 4V to +4V linear voltage ramp
- 50 ms ramp duration
- 100 ms repetition period
- 1 kΩ output impedance

Proposals A and B:

- Square-wave Generator (TTL)
- Level Translation + Buffers
- Ramp Generator

Design Problem B:

- 4V to +4V triangular voltage
- 0.5 duty cycle
- 100 Hz frequency
- 1 kΩ output impedance

Generator Design: Bootstrap Circuit

Capacitor Selection:
- Typically in 100 pF to 1 μF range:
- With low capacitance values, long-duration ramps will require very low (<1 μA) charging currents - R > 1 MΩ!
- If < 100 pF influence of non-linear, stray (parasitic), capacitance + leakage/bias currents affect ramp linearity.
- If > 1 μF, very high discharge current may be required. Select C1 = C2 = 470 nF.

Resistor Selection: (Assume E = +12V)
- As C1 = C2, let R1 = R2 = 10 kΩ (typically) to achieve a nominal required closed-loop amplifier gain of +2.
- \( V_o \) varies from 0V to 8V in 50 ms; \( V_i \) varies from 0V to 4V.
- \( R = \frac{E}{t g \theta} \cdot \frac{V_{max}}{V_{max} - V_{min}} = \frac{(12)(50 \times 10^{-3})}{(470 \times 10^{-3})(4)} = 319 \text{ kΩ} \)
- Choose R = 330 kΩ
Generator Design: Switching Circuit

- Required to discharge $C_1 = 470\,\text{nF}$ from $4\,\text{V}$ to $0$ in $< 25\,\mu\text{s}$.
- Discharge current: $I_1 > (4)(470 \times 10^{-9}) / (25 \times 10^{-6}) = 75\,\text{mA}$
- Required output transistor current:
  - $I_{C2} = I_1 = 100\,\text{mA}$ (≈ $75\,\text{mA}$)
- Assuming $\beta_{2\text{MIN}}$ (or $h_{FE2\text{MIN}}$) = 100:
  - $I_{BMIN} = I_{B1MIN} = I_{B2MIN} = (100 \times 10^{-3}) / (100) = 1\,\text{mA}$
- Hence, the base resistance $r_b = \left[ 5 - V_{BE1} - V_{BE2} \right] / [1 \times 10^{-3}] = [5 - 0.6 - 0.8] / [1 \times 10^{-3}] = 3.6\,k\Omega$
- Choose $r_b = 3.3\,k\Omega$.
- Logic low input compatibility - $V_s = 0.4\,\text{V}$ (1 STTL load = 1.6 mA):
  - $I_s = I_{B1} = \left[ 5 - 0.7 - 0.4 \right] / [3.3 \times 10^3] = 1.2\,\text{mA}$

Semiconductor Device Selection

- Amplifier:
  - FET or BIFET - high $Z_{in}$; very low input bias current (< pA).
  - Slew Rate $S > 8\,\text{V} / 25\,\mu\text{s}$ is $= 0.32\,\text{V/\mu s}$.
  - $f_T = (2)(f_X)$ where $f_X > 1 / 25\,\mu\text{s}$; preferably:
    - $f_T > (2) (10) / (25 \times 10^{-6}) = 800\,\text{kHz}$.
- Transistors:
  - Switching type; high $f_T$, low capacitance.
  - Pulse current capacity $> 75\,\text{mA}$.
- Diode:
  - Switching or Schottky diode.
  - Pulse current capability $> 75\,\text{mA}$.
**Output Stage Design**

- Typically, $R = 10 \, \text{k}\Omega$.
- With this feedback, the output resistance of the amplifier will be very small. Hence $r_o = 1 \, \text{k}\Omega$.
- The required output voltage $V_O$ is given by:
  \[ V_o = V_{RG} - \frac{4}{nR} \]

**Design Problem B**

**Design Specification:**
- -4V to +4V triangular voltage
- 0.5 duty cycle
- 100 Hz repetition period
- 1 k\Omega output impedance

**System Proposal:**
- Square-wave Generator (TTL)
- 0 to 8 V Triangular Generator
- Level Translation + Buffers
Problem B

(a) The circuit on the Figure is used as triangular wave generator.
   I. Describe the performance of this circuit assuming $V_{cont}$ as TTL source.
   II. Sketch the waveforms of $V_{out}$ and $V_{cont}$ for one cycle of $V_{cont}$ (7 marks)

(b) Design the 0 to +8 V triangular generator assuming $V_{cont}$ as 100 Hz, 0.5 duty cycle TTL signal, $\lambda = 0.1 \text{ mA/V}$ and $V_{CC} = 12V$.

(c) Suggest and design a buffer circuit to transfer 0 V to +8 V triangular waveform to -4 V to +4 V signal.

Solution a(i)

(i) Describe performance of this circuit assuming $V_{cont}$ as TTL source,
   At $V_{cont} = 0 \text{ V}$, Q3 is closed as well as Q1 and Q3. Charging current I flows through the D2 and produces positive linear ramp in capacitor.
   At $V_{cont} = 5 \text{ V}$, Q3 is turned ON by the rising base signal;
   The CCS current I flows in Q1 and is mirrored in Q2 and produces negative linear ramp in capacitor.
Solution a(ii)

(ii) Sketch the waveforms of $V_{out}$ and $V_{cont}$ for one cycle of $V_{cont}$

The capacitor voltage falls at a rate of

$$V_c(t) = I \cdot t / C$$

Solution b

(b) Design the 0 to +8 V triangular generator assuming $V_{cont}$ as 100 Hz, 0.5 duty cycle TTL signal, $\lambda = 0.1$ mA/V and $V_{CC} = 12$ V.

- Suppose that the X input is connected to $V_{CC} = +12$ V
- Therefore the current is $I = I \cdot \lambda = 0.1 \times 12 = 1.2$ mA
- The period of $V_{cont}$ is $1/100$ Hz = 10 ms and half period is 5 ms
- Therefore the voltage ramp is 8V/5 ms = 1.6 V/ms
- On the other hand voltage ramp is

$$\frac{dV_c(t)}{dt} = I / C$$

- Thus the capacitance $C$ is

$$C = \frac{I \cdot dt}{dV_c(t)} = \frac{1.2 \times 10^{-4} \cdot 1 \times 10^{-3}}{1.6} = \frac{3.6 \times 10^{-7}}{1.6} = 0.75 \mu F$$
Solution c

(c) Suggest and design a buffer circuit to transfer 0 V to +8 V triangular waveform to -4 V to +4 V signal.

![Buffer Circuit Diagram]

The Integrator Approach

- Miller's Theorem shows that the effect of C on the input is the same as that produced by a Miller Capacitance \( C_M \) across the input terminals of the amplifier, where \( C_M = A \cdot C \).
- Since the overall response is an amplified version of that of a simple low-pass R-C, it is impossible to eliminate slope error.
- Input offset voltage and bias current effects further degrade performance.

Exam Question 1b (2000)

- In the circuit shown in Figure the output voltage of \( A_2 \) is to vary between +5V and -5V with a repetition period of 2ms.
- If \( R_1 = R_2 = R_3 = 10 \, \text{k}\Omega \) and \( R_6 << R_1 \), derive an expression for the periodic time of the output waveform and, hence, determine suitable values for \( C_1 \) and \( R_4 \) if the connection to \( R_1 \) is set at the mid-point of \( R_6 \). State clearly any analytical assumptions made.

![Exam Question Circuit Diagram]

Notes
Solution

- Consider first the output stage. Diode assumed ideal $V_d = 0\, \text{V}$.
- If $D_3$ is ON then
  \[ \frac{V_o - R_4}{R_4 + R_5} = \frac{15 \cdot R_5}{R_4 + R_5} \]
- If $V_o = 5\, \text{V}$ then $R_4 = 3 \cdot R_5 = 30\, \text{k}\Omega$.
- The output voltage of $A_1$ must vary in range $\pm 5\, \text{V}$. (As voltage $V_o$ is $\pm 5\, \text{V}$ and $A_2$ switches at 0V). If $R_2$ is set to provide an input is the integrator of $\beta V_o$.
  \[ \frac{\beta \cdot V_o}{R_1 \cdot \frac{R_1}{C}} \]
  for $t = T/2$, i.e.
  \[ T = \frac{2 \cdot R_1 \cdot C_1}{5 \beta} = \frac{4 \cdot R_1 \cdot \frac{R_1}{C}}{\beta} \]
- If $\beta = 0.5$; $T = 2\, \text{ms}$ and let $R_1 = 10\, \text{k}\Omega$, i.e.
  \[ C = \frac{R_1}{4R_1} \cdot \frac{0.5 \times 2 \times 10^{-3}}{4 \times 10^{-4}} = 25\, \text{nF} \]

Exam Question 2b (2003s)

- The switch $S$ in the circuit shown in Fig. 2 changes from position 1 to position 2 when the output voltage $V_o$ falls to -8 V. The switch returns to position 1 when $V_o$ rises to +8 V. Using superposition or otherwise, derive an expression for the capacitor charging current for each position of the switch, sketch the output voltage waveform $V_o$ and determine the frequency of oscillation of the circuit given that $R = 50\, \text{k}\Omega$, $C = 10\, \text{nF}$ and $E_+ = +4\, \text{V}$.

[15 Marks]