The Engineering Council Examination Part 2 (c)

Waveform Generator with IEEE -488 Interface .

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Waveform Generator with IEEE -488 Interface .

1. Introduction :

1.1 Description:

The IEEE-488 interface is a standard parallel interface used in the control of instrumentation. This interface is typically used in the test and measurement systems.

In 1965, Hewlett-Packard designed the Hewlett-Packard Interface Bus (HP-IB) to connect their line of programmable instruments to their computers. Because of the high transfer rates (nominally one Mbytes/s), this interface later was accepted as the IEEE Standard-1975. This has evolved to ANSI/IEEE Standard 488-1-1987. Today the name the General Purpose Interface Bus, GPIB is more widely used than HP-IB.ANSI/IEEE 488-2-1987. Thus strengthened the original standard by defining how controllers and instruments communicate with each other. Standard commands for Programming Instruments (SCPI) took the command structures defined in IEEE 488-2 and created a single, comprehensive programming command set that is used with any SCPI instrument. The PC can then be used to control and transfer bi-directional data for test and measurement instruments.

1.2 Background :

The MAX038 is an integrated circuit, which can produce triangle, sawtooth, sine, and square and pulse waveforms. It became necessary to produce a piece of equipment to demonstrate the principles of how this integrated circuit, function generator could be interfaced to the PC and controlled using software on the IEEE-488 bus.

1.3 Objective:

(a) To design and build a waveform generator consisting of hardware built around the MAX038.

(b) Interface this to the IEEE-488 general-purpose interface (GPIB).

(c) Analyse the waveforms generated and compare with theoretical results.

(d) Investigate Total Harmonic Distortion (T.H.D.)

1.4 Work Involved :

(a) To design and build a suitable interface card to interface the waveform generator board to the IEEE-488 bus.

(b) To build the Waveform Generator Board which will consist of the High-Frequency Waveform Generator integrated circuit, MAX038.

(c) To write the program using HP-VEE software.

1.5 Instrument Program Objective:

(a) To create an instrument driver for the Waveform Generator board.

(b) To create a user interface that will allow the Waveform Generator to be controlled via controls and pull up menus.

(c) To build an application program to operate the Waveform Generator using HP-VEE.

2. Background to work carried out:

2.1 *System Design* :

The project brief was to design a GPIB controlled waveform generator using the MAX038, high precision function generator integrated circuit. Waveforms could be created at a frequency range up to 20MHZ. Figure 1 shows the overall system block diagram.

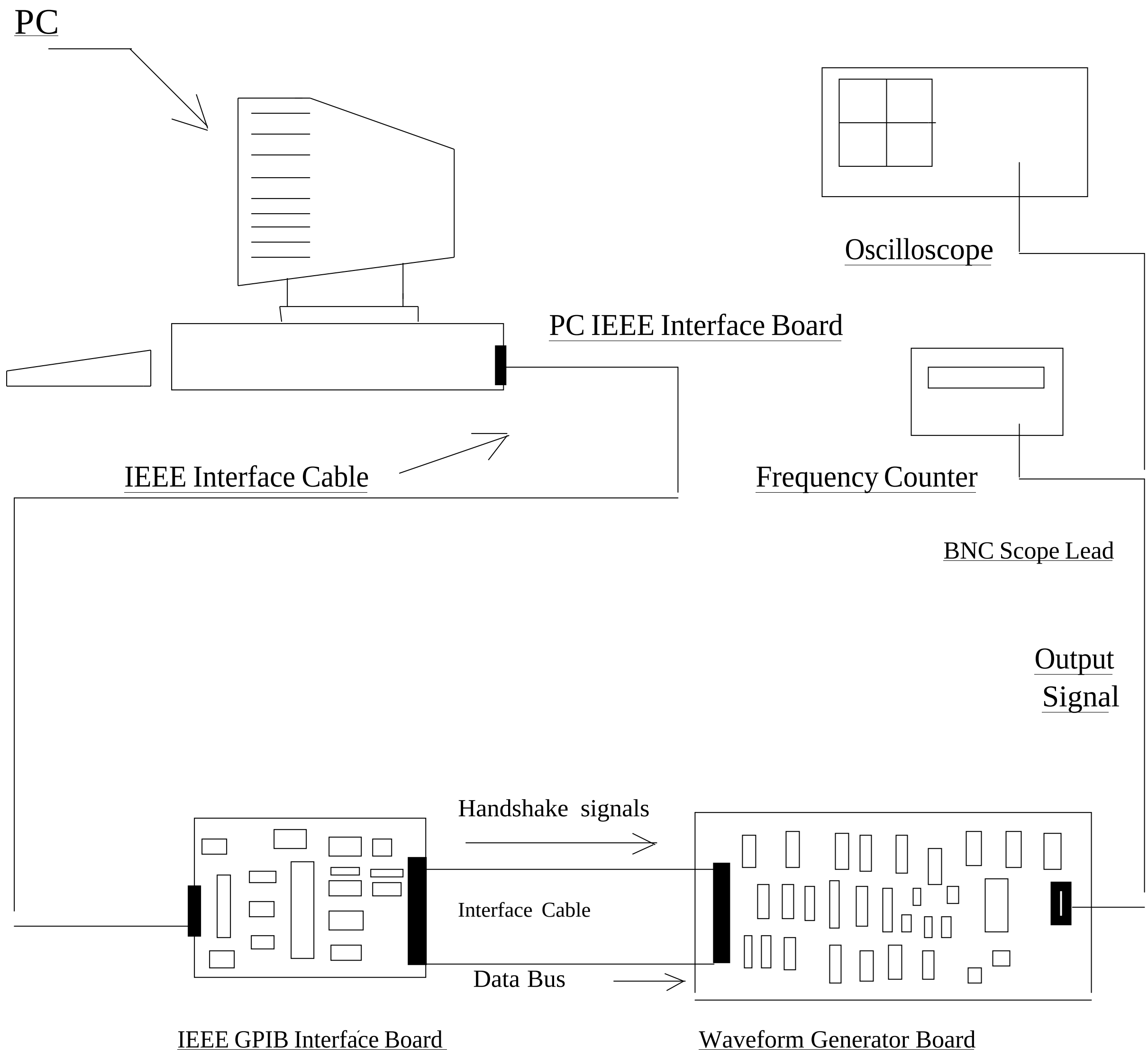

figure 1

2.2 Function Design:

A computer with an IEEE interface card is used as the controller. The interface card is supplied with software routines to communicate with the GPIB bus. The software provides binary language interface files which allow programs to be written in BASICA, QBASIC, BASIC, and Microsoft C. A software development system for instrument control and data acquisition used to develop the application program for the Waveform Generator board will be used. This will be the HP-VEE Operator interface system.

3. *The General Purpose Interface Bus (G PIB):*

3.1. Function:

The GPIB is a byte-serial bit-parallel asynchronous system using a three-wire handshake technique. The GPIB standard allows for 32 devices, with maximum transmission length of 20 metres, with no more than 2 metres between each device. A maximum transfer rate of one megabyte per second is possible. The rate automatically adjusts to the speed of the slowest device. Each device is assigned a GPIB address so that the controller can send and receive commands and messages for each device. Messages can be sent or received between each device. These devices are normally test instruments such as an oscilloscope, a function generator frequency counter as well as the GPIB interface board. The controller is normally the PC, the listeners and talkers are usually the test instruments i.e. the devices that are to be controlled. DIP switches located usually at the rear of the instrument set up the unique IEEE-488 address for the instrument.

There are three categories of instruments used.

Controller: Provides commands that cause a device to perform a task. It is a talker and a listener.

Talker: Transmits data over the bus either asynchronously or in response to a command.

Listener: Receives data over the bus either asynchronously or in response to a command.

Bus Structure.

The GPIB bus is made up of 24 lines of which 16 are active. Of these, 8 are data lines, 5 are bus management lines and 3 are byte transfer lines.

Data lines : 8 bi-directional lines used to transfer information from device to device. The data is normally transferred in 7-bit ASCII format.

Bus Management Lines: 5 unidirectional lines used to manage the orderly flow of information across the interface.They are described as follows:-

ATN : Attention ; used by the controller to indicate whether information on the data bus is device information or a control message.

IFC : Interface clear ; used by the controller to reset the interface into a quiescent state.

REN : Remote enable ; places a device in a remote state.

SRQ : Service request ; indicates to the controller that it requires attention.

EOI : End or Identify ; indicates that the current byte is the last in a sequence.

Byte Transfer Lines : These lines are used to coordinate the transfer of data over the bus.

DAV : Data Valid.

NRFD : Not ready for data.

NDAC : Not data accepted.

The GPIB bus a negative logic system, which allows the system to be designed with open collector outputs. This allows the bus lines to be connected in parallel.

Data Transfer Timing

Figure 2

The sequence of transfer of a byte of data over the bus is shown in figure 2. The sequence is as follows: Initially the source checks for a listener and places data on the GPIB bus.

t - 1 : All acceptors ready and NRFD goes high with the slowest acceptor.
t 0 : Source validates data, i.e.,sets DAV low.
t 1 : First acceptor sets NRFD low, i.e., not ready for data.
t 2 : NDAC goes high with the slowest acceptor to indicate all acceptors have accepted data.
t 3 : Source sets DAV high i.e., data byte is no longer valid.
t 4 : First acceptor set NDAC low in preparation for next cycle.
t 5 : Next cycle begins.

3.2. Hardware Design :

The GPIB interface board was designed around the HEF4738V IEC/IEEE interface controller manufactured by Phillips. Other controllers that could be chosen are the MC68488 by Motorola or the 8291 and 8292 from Intel.

The HEF4738 was chosen because no controller functions are required. The HEF4738 implements the basic listener and talker functions of the IEEE-488 standard. It provides two wire hand shaking for input and output data transfer.

3.3. *Circuit Design .*

Figure 6 on page 10 shows the schematic diagram of the GPIB interface board. The layout of components is shown on page 24. Operation of the GPIB board requires 4 support circuits.

1) Power up :

The Ipon (input power up) pin must be kept low for at least 32 clock periods, the high for at least a further 32 periods, before it is forced low again in order to initialise the HEF4738. This is required to load the setup data into the serial input Isr from the DIP switch settings. This is implemented using a RC network and U9, a 4093 IC.

2) Set-up and Addressing :

Parallel in serial out shift registers are used to set up the HEF4738 (U7 and U8). The following data is set on the DIP switches (SW1 and SW2) and loaded into the Isr pin. Figure 3 shows the Dipswitch settings for the GPIB board.

A5 - A1 : The unique device address on the bus.
ton : Talk only.
lon : Listen only.
lt : Listen and talk subset.
rsv : Request for service
rtl : Return to local.
ist : Individual status

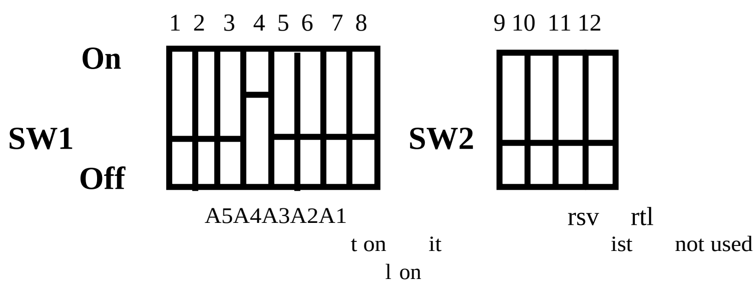

figure 3

3) Bus Transceivers:

Bi-directional inverting transceivers are used because the HEF4738 operates on positive logic and needs to send and receive data. U1 to U5 are 74LS242 and are controlled by GBA and GAB.

a) Bus management Lines: (IFC, ATN, REN, EOI)
These lines are always inputs, so the transceiver is configured permanently as A=input and B=output. The schematic diagram of figure 6 on page 10 shows U1 set up in this manner.

b) Handshake Lines : (NRFD, NDAC, DAV)
Two transceivers are used, a talk (U2) and a listen (U3). The direction is controlled using two signals, Ota (output talk) and IATN. Ota is HIGH when the device is a talker and LOW when it is a listener. IATN is LOW when the device is in DATA MODE and HIGH when in COMMAND mode. By inverting IATN and NAND-ing with Ota, direction control is obtained. This is done using nand gates U6a,U6b and U6c, a 4011 IC, to create signal (DCS).

C) Data Lines: (DI01 . . . . . . DI07)
The direction of these lines is changeable depending on the flow of data. Two transceivers, U4 and U5 are controlled by DCS.

4) 2 MHz Oscillator :
The HEF4738 requires a 2 MHz clock to operate at it's optimum speed. The IEEE controller works quite well with a 1 Mhz crystal controlled oscillator module, which was more readily available, and so was used.

3.4. *Device Listener Handshake* :

The device listener handshake lines are Odvd and Irdy- (Data to device valid and ready for next byte). These are used for two-wire handshake procedure. Figure 4 shows the timing of these signals with respect to the interface handshake. If the device reacts with sufficient speed, signals Odvd and Irdy- can be connected together and are able to:

a) Accept a new data byte within one clock period after ODVD goes high.
b) Be ready to accept the next data byte within two clock periods plus the minimum settling time of the talker device at all times.

Figure 4 - Timing diagram showing the relationship between device listener handshake and interface acceptor handshake. For the design of the GPIB interface board which will control the waveform generator board,the conditions are met so that Odvd and Irdy can be connected together

Note : For more information on the HEF4738 see the PHILIPS data book " HEF4000 Logic Family " IC04 1990

4. *Work Carried Out:*

4.1 *EASY-PC :*

The GPIB board layout was done using EASY-PC. This drawing package is the most recent method of creating and editing PCB layouts and circuit schematics. Easy-PC replaces the old method of stick-down pad and tape or stencil methods. Easy-PC requires the use of the PC 386/486 running DOS 2.0. A minimum memory of 512K is necessary. Easy-PC contains libraries of components and symbols and ability to create and modify new symbols and components.

The GPIB board layout was designed by selecting a Eurocard from the PCB library. The following lists the stages for designing the layout.

a) Select PCB layout.
b) Select a Eurocard from the PCB library.
c) Select and position 96-pin Eurocard connector, P1
d) Select and position 26-pin connector, P2
e) Select ICs starting with a 40-pin DIL for HEF4738 and continue with the 16,14,and 8pin DIL symbols.
f) Select Pads and Vias and place in appropriate positions.

g) Track layout began with the power supply rails, i.e. the 5V and Ground lines. It was decided to put the ground line on layer 8 and the power line, 5V on layer 1 and to use the perimeter of the board as much as possible. This would facilitate having as much space as possible to run the signal lines, and also reduce signal noise.

h) Now the tracks for the signal lines could be laid. This involved a lot of tedious work where editing and changing between bottom and top layer, (layer 1 and layer 8) was required to fit the entire network of tracks on the space available.

I) Text could now be put on the PCB to make the board cosmetically attractive and professional.

J) Finally the layout was saved and a backup created. The AutoSave feature would be in operation throughout.

The file was saved as GPIB.PCB.

4.2 *The Building of the GPIB Board*

4.2.1 Easyplot and Print.

A double-sided version was used. The PCB layout for layer 1 and layer 8 was printed out separately on sheets of transparent PCB paper, known as Acetate.This was done using the print option from the menu of Easy-PC to a laser printer.

4.2.2 Manufacturing the PCB:

A Photo-Resist copper clad board was used as the PCB. This is a double sided copper clad board and consists of laminated material of woven glass fabric bonded and heat cured, flame resistant epoxy resin. The copper is clad with photo-resist.

The PCB was made using the following procedures:

- **THE LAYOUT MASK:** The layout of both sides of the PCB was printed on acetate paper using the laser printer and by choosing the print option on easypc

- **EXPOSURE:** This was done by placing the board in an ultraviolet exposure unit and exposing both sides of the laminated board contained between the sheets of acetate for 2 minutes.

- **DEVELOPMENT:** The laminate was then immersed in developer solution and gently washed until the photo-resist that had been exposed is removed. The mask of the layout was then seen on both sides of the laminated board.
- **ETCHING:** After a post development check for faults, the board was immersed in ferric chloride solution contained in an etching bath and sprayed until the unwanted copper was removed.

The exposure and development procedures were then repeated to remove the photo-resist from the layout. The board was then cut to eurocard size, shown as a border around the layout. The manufacturing process of the PCB was now complete.

The PCB was then drilled and components inserted and soldered. Feedthroughs had to be inserted between the layers using the vias to create a connection between the front and back layer. This was done using strands of wire cut to size and inserted and soldered on both sides of the vias of the PCB. The PCB was now ready to test.

4.3 *Testing the GPIB Board*

The GPIB board was now connected to the IEEE-488 bus. This is done using the IEEE-488 cable, which was connected between P2 and the connector of the IEEE-488 interface board located at the rear of the PC. A 5V-power supply was also connected to the GPIB board.

Selecting “instrument finder ”, and selecting “HP32840 or HP82341 HP-1 at select code 7” a menu of all addresses from 700 to 731 was displayed as addresses seen by the PC. The dipswitches were set for address 702.

A5 = on, rest off are set on the GPIB board.

Binary data was sent out to the board using a HP-VEE test program in the form of 00, AA, 55 and FF to ensure the correct operation. The Logic analyser was used to monitor the data bus on the GPIB board. Using the clock on the board and triggering on the falling edge of ‘ATN’, the data transfer could be seen. This program is shown in figure 5 below.

Figure 5 Test HP-VEE Program for GPIB board

Figure 6 Schematic of GPIB Board

5 *The Building of the Waveform Generator Board*

5.1 *Work Car ried Out:*

The first stage in designing the PCB from the schematic layout was to first build a prototype using matrix board and fixing the components using wire-wrapping techniques. Insulated fine wire was used to join pins and sockets especially manufactured for this purpose. A wire-wrapping gun was used to wire-wrap strands of insulated wire of various colours to the components. The different colours were used to represent the different signal lines. For example, red represented +5V and black represented 0V. Remaining colours represented the signal lines. Wire wrapping is the best method for building prototype boards because mistakes can be corrected and changes in design can be made by simply uprouting and rerouting the wires.
In general wire-wrapping prototype circuit boards is widely used as a method of manufacture by design engineers. Once the prototype is built and tested, the PCB can be designed using Easy-PC.

5.2 *Description of the MAX038 Integrated Circuit:*

The MAX038 is a high frequency, precision function generator that can produce accurate low frequency to high-frequency waveforms. These waveforms can be sinusoidal, square, triangle, saw-tooth and pulse. Minimum of external components is required to form the complete circuit. The data sheet for the MAX038 was obtained from RS Components.

5.3 Interfacing the MAX038 to the GPIB Board:

The Waveform generator board can be divided into three main sections

a) The Decoder Board

b) The Digital to Analogue Converter Circuits.

c) The MAX038 Waveform Generator Circuit.

5.3.1 The Decoder Circuit:

The MAX038 had to be controlled to gave a variation of

a) Frequency.

b) Amplitude Adjust

c) Waveform type (Sinusoidal, Square, Triangular)

d) Duty-cycle (Saw-tooth and Pulse Waveforms)

e) Fine-Frequency

f) Range of Frequency

Four control signals interface the Waveform Generator board to the GPIB board. These are Oclr, Irdy, Odvd and ATN-. Irdy and Odvd are tied together since the handshake timing is not critical. Oclr is not used.

ATN- is a command signal when high and data transfer signal when low. A counter 74LS160 (U1) and a 3 to 8 line decoder, 74LS138 (U2) are used to decode the 6 control signals required to enable data registers for the storage of digital code to carry out each function. The control signals co-ordinate the data information into the correct data registers.

5.3.2 The Reset Circuit:

The reset circuit consisting of R1, C1 and D1 causes the board to reset on power up. The delay time to initialise is approximately 2.2R1C1, since 2.2RC = the time for a capacitor to charge between 10% and 90% of the its final value of voltage through a resistor. U4 and U5 are used to reset the counter U1. A reset switch is added so that the counter can be manually cleared. This is necessary because indeterminate operation can occur.

Figure 7 Sheet 1 Schematic of Waveform Generator Board

Figure 8 **Sheet 2 Schematic of Waveform Generator Board**

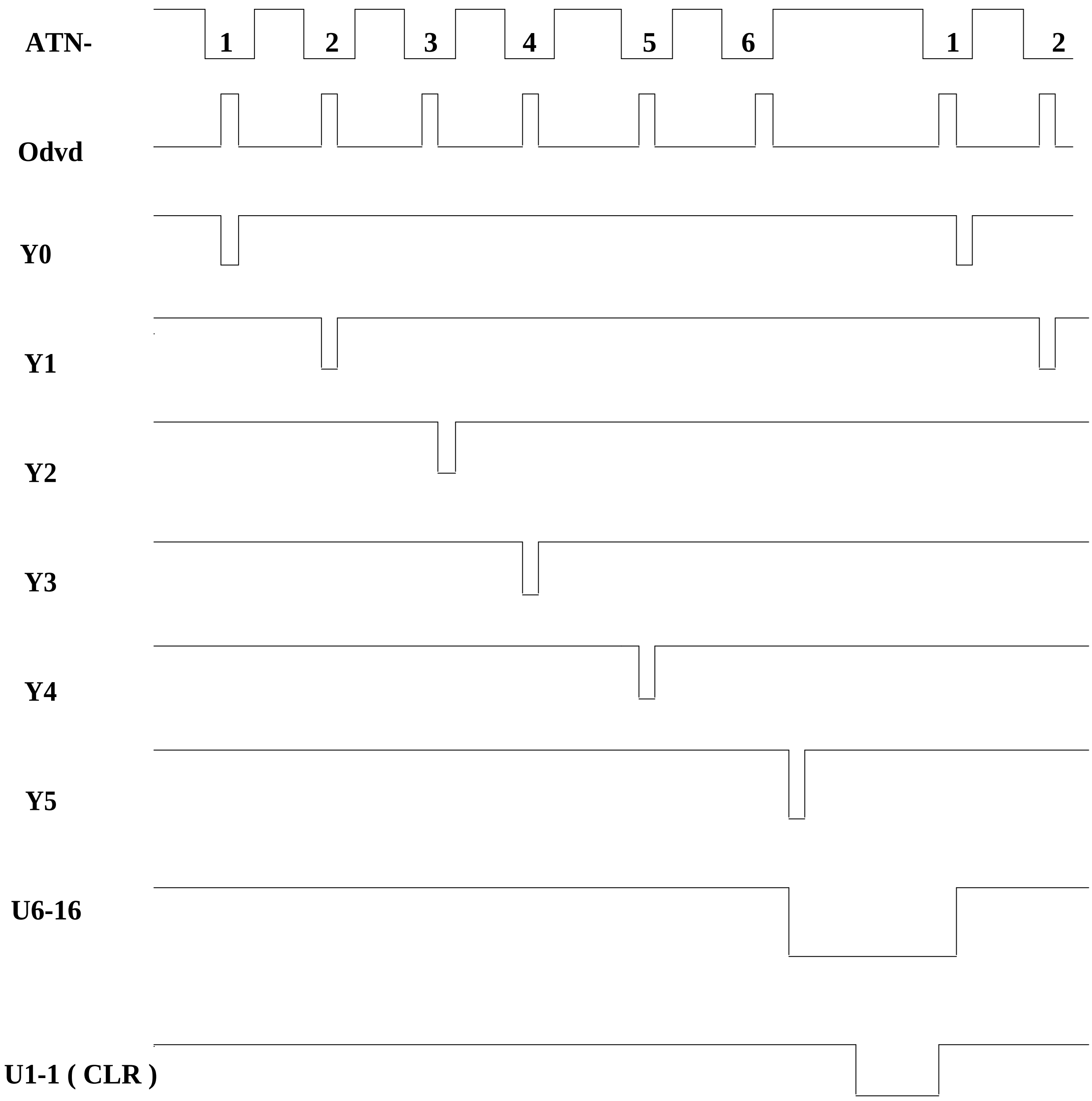

Figure 9

Each time the program sends a command to output a byte of data, ATN- goes high. ATN- goes low after the command has set up the IEEE-bus to transfer a data message. Later an odvd pulse indicates data is being sent. Odvd is used as the clock to the counter (U1). The level triggered latch, U6 and using a combination of logic gates, U4 and U5, cause the counter to reset the count to zero after the sixth data byte has been transferred. The cycle can now start all over again.

For each count of the counter,U1 the 3 to 8 line decoder decodes the count on the ABC inputs and sets the relevant Y output low. ATN- resets the counter after Y5 goes low and latched by the U6. The output U6 stays low until after ATN- goes high and goes high when odvd is high on the beginning of the next cycle.

5.3.3 The Digital to Analogue Control Circuits:

U3 and U5 invert the outputs of the 3 to 8 line decoder. The six control signals latch six bytes of data in storage registers that set up the digital inputs to the D/A converters.

a) The Wave Select Latches:

The data latch 74LS74, U7 stores data for A0 and A1 using only D1 and D2 of the data bus. A0 and A1 go directly to the wave select inputs of the MAX038.

b) Range Select:

The Range select is set up by data latch U5a and U5b shown on sheet 2 of 2. Four ranges are set up using a 74LS74. Four ranges are sufficient to cover the full bandwidth of the MAX038.

Sheet 2 of 2 contain U1 to U4, to store digital data for four of the functions necessary to control the MAX038

c) **Frequency Select**: This signal latches the frequency byte in the data latch U1.

d) **Duty-Cycle Select:** This signal latches the duty-cycle byte in data latch U3.

e) **Fine Frequency Select:** This signal latches the fine-frequency byte in data latch U2.

f) **Amplitude Select:** This signal latches the amplitude byte in data latch U4.

The level of digital range is from 0 to 255 for c, d, e and f so that there is a resolution of 256 bits.

5.4. Programming the MAX038 Circuit :

5.4.1. Frequency Adjust:

The digital to analogue circuit for coarse-frequency is shown in figure 14 and uses a constant current source to drive the MAX038 at IIN. IIN has to have a range between 2µA to 750µA to gave a range of frequency between a minimum value and a maximum value.

The fine-frequency input, FADJ control is set up to vary between –2.4V and +2.4V.

The Duty-cycle input, DADJ control is set up to vary between –2.3V and +2.3V.

COSC on Pin 5 is the capacitor, which sets up the frequency and is inversely proportional to the frequency.

The output frequency is determined by the current into the IIN pin, the COSC capacitance (to ground), and the voltage on the FADJ pin. When VFADJ = 0 the fundamental frequency is given by the formula:

$$F_o\,(MHz) = I_{IN}\,(\mu A) / C_f\,(pf) \qquad \mathbf{1}$$

The period is given by:

$$T_o\,(\mu s) = C_f\,(pf) / I_{IN}\,(\mu A) \qquad \mathbf{2}$$

Where:

IIN = current injected into pin 10 (between 2µA and 750µA)

Cf = Capacitance connected between Cosc and GND (20pf to > 100pf)

An op-amp circuit and a constant current source is used to set up frequency adjust. A 2.5V reference from the MAX038 is used as the reference to the D/A converter circuit. Since a voltage reference rather then a current reference is needed, the current output is converted to a voltage output using the op-amps, U18 and U19. The constant current source circuit consists of op-amps U11a and U11b, the MAX412 and transistors Q1 and Q2 with associated resistors.

The constant current can be varied between 2µA and 750µA. By changing the voltage between 0 and 2.5V in proportion to the digital inputs, 256 frequency values can be set up. The 2.7MΩ resistor limits the constant current to 2µA for a digital input of 00Hex and the 3.3KΩ resistor limits the constant current to 750µA for a digital input of FFHex.

5.4.2. Fine-Frequency adjust:

To limit FADJ and DADJ to 250mA, 10K resistors are used in the circuit. FADJ modulates the fundamental frequency when VFADJ varies between ± 2.4V. This changes the fundamental frequency to between ± 70% of its value. FADJ has a constant current sink of 250µA and is furnished by a voltage source of 2.5V from pin 1 of the MAX038. This current sink into FADJ is controlled by the fine-frequency control from U13. The mid range of VFADJ of 0V is set up by a digital input of 80Hex or binary 128. R9 adjusts the range of VFADJ to between +/- 2.4V. When VFADJ increases to + 2.4V the current source is from U13 caused by a low digital input to the D/A converter. Alternatively when U13 is being driven by a current from the D/A converter due to a high digital input, the op-amp output goes low draining current away from FADJ causing VFADJ to drop towards – 2.4V.

D8 is latched in a separate F/F (U8a) so that on reset and on power up the digital input is never too high to over drive the MAX038. The +/- 70% values of digital data only change between +/- 70% of the digital bit range so that:

Fine-Frequency digital adjust is = -70 % < 128 < + 70 %

5.4.3. Duty-cycle Adjust:

DADJ is designed in the same way as FADJ but using U15 to control the input to pin 7 of the MAX038. R19 and trimmer, R13 are selected so that the adjustment can be between +/- 2.3V. The circuit is designed to vary over the full 256-bit range.

Duty-cycle digital adjust = 0 < 128 < 255

5.4.4. Amplitude adjust:

The output waveform comes from pin 19 of the MAX038 and is 2V peak to peak. This can be amplified by summing the output signal to the converted digital output of U10 using the video amplifier, U16. Since the voltage reference of the AD7523 constantly changes with the amplified output of U16, the digital inputs to the circuit will cause the output to amplify or attenuate. The LM6362 high-speed operational amplifier delivers 300 V/µs and has a 100MHz-bandwidth product.

The output amplified waveform is fed to a 50Ω 50 MHz low-pass filter to limit high frequency noise.

5.4.5. Range adjust

A bandwidth of 10MHz is obtained by switching capacitors and using the constant current source to control IIN.

The latch U5a and U5b provide 1 of 4 different codes that are decoded by U6, a 3 to 8 line decoder. The outputs are used to select one of 4 capacitors that are switched into cosc at pin5 of the MAX038. Relays, RL1, RL2, and RL3 switch Range 2,3 and 4.with capacitors C7, C8 and C6 respectively.

The frequency ranges is shown in Table 1 below

Table1

1	250KHz to 10MHz	33pf	C9	0	0	
2	17KHz to 1MHz	1033pf	C7+C9	0	1	
3	550KHz to 26KHz	3033pf	C8+C9	1	0	
4	20Hz to 1KHz	1000033pf	C6+C9	1	1	

5.4.6 Waveform Select:

Storing data bits D1 and D2 in U7a and U7b, the 7474 latch can select four different waveforms. By latching 00,10 or 11,and connecting the outputs to A0 and A1 of the MAX038, a square, triangular or a sinusoidal wave can be formed. The circuit is on sheet 1 of the schematic of the waveform generator board.

6. SOFTWARE DESIGN:

HP-VEE is a software development system for data acquisition and instrument control. The writing of software is easy for controlling instruments via the GPIB bus. Tedious low level GPIB commands are replaced by icons,panels and control boxes. HP-VEE presents the user with a Microsoft QuickBasic or C program development shell along a set of mouse driven options, with dialog boxes and menus.

HP-VEE produces a front panel for the instrument. All frequency, duty-cycle and amplitude changes can be made using slider icons on the computer screen. Figure 10 shows the complete layout of the HP-VEE program for the Waveform Generator.

6.1 Program Description:

The program is built using a flowchart system where there is a start and an end. To draw the layout of the program the objects are selected from menus located in a toolbar at the top of the screen.

The object **'Start'** is selected first, and then **'for count'**. The **For Count** panel has a number which can be changed with the mouse or keyboard and determines the number of cycles the program will run.

The **device driver** for the waveform generator board is **'newDevice (@ 702)'** by selecting **'New Instrument'** from the toolbar menu. The name 'newDevice' indicates that the device is not one of the standard instrument drivers already installed. In this case, the GPIB board is the instrument to be driven and the address is set on Dipswitches. The address for the GPIB board is found as 702 by using 'instrument finder' icon in windows and setting the dipswitches to address 02.

Slider collectors provide the data for Frequency, fine-frequency, duty-cycle and amplitude. Radio buttons provide a choice of the three waveforms, 1 = sine wave, 2 = square, 3 = triangular wave.

The **Call Function** panel is a **user object** panel and is similar to the main layout panel, much like a interrupt routine in a flowchart program. The user object panel is independent of the main panel and is a panel on the main panel. Figure 11 in the appendices shows this panel expanded. The **user function** panel contains 4 device drivers with bytes, 00, 01, 10 and 11 for range 1, 2, 3, & 4.

The **SELECT** panel in conjunction with the radio buttons compare 1, 2 or 3 with byte 01, 10 or 11 and output the byte matched to **'newDevice@702'**.

The **FREQ FINE ADJUST** panel in conjunction with the **% FINE ADJUST** slider compares between –70% and +70% of the frequency range with byte values and when a match is made outputs the byte to the '**newDevice@702'**. Inside this UserObject panel there are 140 **If/Then/Else** panels, each threaded to a '**newDevice@702'** driver panel.

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The range starts at –70 outputting byte 58Hex (00111010). Mid range at zero outputs byte 128Hex (10000000) and +70 outputs byte 198Hex (11000110).

The **Press For** panel is an independent panel. When the button **Info About** is pressed using the mouse, the panel expands and text describes the representation of the wave and range select buttons.

The **Bus I/O Monitor (hpib7@ 7)** is an independent panel that displays a view of data on the GPIB bus. The panel shows both the binary output and the ASCII character. The panel can be scrolled backwards and forwards to display data information in the same way as a logic analyser.

Note: The objects are threaded together so that the flow of the program allows the device drivers to be concurrent with the register layout of the waveform generator board.

The program can be run using the **START** button or the **Run** button at the top right of the screen, and can be stopped anytime using the **Stop** button.

Figure 10 **Master Layout of HP-VEE Program**

7. System Tests:

7.1 Program Execution :

Using a selection of capacitors and taking frequency measurements until maximum bandwidth was obtained tested the system. The inputs FADJ and DADJ to the MAX038 were measured using the minimum and maximum values on the slider controls. By adjusting R9 and R13 the range of VFADJ and VDADJ was set for ± 2.4V and ± 2.3V respectively. The maximum value of IIN for frequencies adjust was 650μA. The maximum frequency obtained was 10MHZ but with fine-frequency slider adjust this frequency could be fine-tuned to 13MHz

The full set of readings for frequency is shown in the appendix.

The frequency range limited the bandwidth product and amplification was not possible beyond 2MHz. The full scale of the amplitude slider could not be used because of clipping of the output waveform. A compromise was made to obtain the maximum bandwidth product by using a selection of capacitors to set up a reasonable frequency range and yet demonstrate the amplification of the output signal.

By varying the duty-cycle slider on square-wave, a pulse waveform could be formed generating pulse waveforms from 15% to 85% of the fundamental waveform. Selecting triangular waveform by pressing **Radio button 1** and varying the duty-cycle generated a saw-tooth waveform.

The amplitude could be varied by using the amplitude adjust slider. The slider at setting zero was maximum amplification and at adjustment 255 was unity. Increasing the digital output attenuated the output signal. When D01 to D08 was FFHex the gain was unity. When D01 to D08 was 00Hex the output signal was at maximum gain.

The output waveform was 2V peak-peak from pin 19 of the MAX038. This waveform could be amplified by U16, LM6362 from a gain of unity to a gain of 12. Setting the slider adjustment to 255 set a gain of 1. Decreasing the adjustment to 70 set a gain of 12. Any adjustment below this value saturated the LM6362 causing clipping of the output signal to occur.

7.2 Quality of the output signal:

7.2.1 Slew rate:

The slew rate was measured by setting up a 1MHz square-wave signal so that the output saturated at 25V pk-pk. The slew rate was measured to be 200V/μsec. This compares favourably with the data sheet for the LM6362 that states a slew rate 200V/μsec for the amplifier. It was not possible to measure the slew rate by saturating the amplifier at low frequencies. The slope of the waveform was very sharp and perpendicular and a measurement could not be obtained on the oscilloscope.

The slew rate was measured for a sinusoidal wave at a frequencies and amplitudes as shown. The waveform generator should have minimum slew rate of 2πAf Volts/sec for an output signal.

A= amplitude in volts π = 3.14,f = frequency in herz.

Frequency, f	amplitude, A	Slew rate Volts/μ sec	2πAf
1KHz	12V	0.083	0.075
1KHz	5V	0.031	0.031
1MHz	12V	67	75
1MHZ	5V	25	31

Table2

7.2.2 Total Harmonic Distortion:

Total Harmonic Distortion measures the purity of the waveform with reference to a sine wave. A distorted waveform puts harmonics into the system being tested by introducing multiples of the fundamental frequency. THD is measured in terms of the harmonic content of the wave.

A Kenwood Audio Distortion Meter was used to measure the percentage harmonic distortion of 100Hz, 1KHz and a 20KHz sinusoidal waveform.

Frequency	THD %
100Hz	4.5
1KHz	4.5
20KHz	3.6

Table3

The distortion rate given in the data sheet for the MAX038 is 0.75% with duty-cycle adjusted to 50% and 1.5% with duty-cycle unadjusted. A test bench function generator gave a reading of 0.5% when tested.

8. *Summary:*

8.1 Conclusion:

The MAX038 GPIB waveform generator illustrates how the PC can be used to control an interface on the IEEE-488 bus. The waveform generator board and GPIB board is an instrument that can be used in a laboratory environment. The HP-VEE program illustrates the use of panels and objects in a graphical presentation to create a program that is understandable to the user who has no knowledge of software engineering.

The quality of the output waveform is dependent on the MAX038 because the IC is the heart of the system. The accuracy of the output waveform is dependent on the tolerances of the components and on the amount of stray capacitance. The project does not demonstrate the full frequency range of the MAX038 that should operate up to 20MHz. The frequency readings are not altogether accurate to the theoretical calculations. Some accuracy is obtained at low frequencies but the high frequency ranges are programmed by stray capacitance and the resistance introduced by the relays.

The main conclusion means that the project works well as a waveform generator but cannot be compared between a theoretical and practical representation. The limitations of the MAX038 are more apparent at low frequencies. Since a sine wave is formed from a triangular wave, this becomes more obvious at low frequencies, especially below 100Hz. High frequency noise and bandwidth limit the quality of waveforms at very high frequencies.

8.2 Recommendations:

a) The next procedure would construct the waveform generator on a PCB.

b) Low impedance ground plane and connect all five GND pins directly to it.

c) A 50Ω 50MHz, Lowpass filter is recommended for the output to filter out high frequency noise.

d) Fast CMOS switches can be used instead of relays.

e) The MAX442 amplifier capable of driving a 50Ω coaxial cable could be used to buffer the output.

f) Bypassing V+ and V- directly to the ground plane with 1μf tantalum capacitors in parallel with 1nf ceramics and keep leads short to minimise inductance.

g) Minimise trace area around cosc to reduce parasitic capacitance.

The above suggestions would increase the quality of the output waveform, increase the frequency range and eliminate most of the stray capacitance and inductance associated with the wire-wrapped board.

Three Eurocard PCBs would be required with ±5V and ±12V Power supply and all installed in a Eurocard box

9 *Appendices:*

Figure 11 Expanded Layout of Waveform Select and Fine-Frequency Adjust

Figure 12 Panel Functions Frequency readout of Drop Down List

Range 1, 2, 3 & 4

The **Edit** function of the toolbar menu allows the user to insert **breakpoints** and to select **'Animate'**. Animate causes a 'highlight' to appear on the thread or object and follows program progression.

Figure 13 Layout of GPIB and Waveform Generator Boards

10. References:

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HP-VEE Reference Manual

Maine A.C. **Interfacing Standards for Computers**

National Instruments **Measurement and Automation Catalogue 1999**

National Semiconductor **LM6162 High speed Operational Amplifier**

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Waveform Generator with IEEE -488 Interface

11 Abstract:

The aim of the project was to interface the MAX038 Waveform Generator integrated circuit manufactured by MAXIM to the IEEE-488 bus. The MAX038 is a stand-alone waveform generator that can create sinusoidal, square, triangular, saw-tooth and pulse waveforms with a minimum of external components.

All software would be created using a graphical programming package designed by Hewlett Packard called HP-VEE. The objective was to control the operation of the MAX038 from the PC using the waveform generator as an instrument on the IEEE-488 bus. The project consists of two boards, the General-Purpose Interface (GPIB) board and the Waveform Generator board.

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The Waveform Generator has the facility to form five different waveforms in which frequency, fine-frequency, duty-cycle, range, and amplitude can be adjusted by the HP-VEE software program. Eight-bit digital messages produced by the HP-VEE program drive the MAX038.

The MAX038 integrated circuit can produce a sinusoidal wave, a triangular wave or a square wave by receiving a coded message from the HP-VEE software program. A saw-tooth and a pulse waveform can also be formed in this way.

The software to drive the Waveform Generator was designed using graphical panels, icons and object sliders on the PC. The HP-VEE creates a front panel instrument driver for the GPIB board. Linking graphical images of functions created a program to drive the waveform generator board.

The Waveform Generator board was connected by way of the GPIB board to the IEEE-bus. The HP-VEE software program on the PC could then control the system.

The Waveform Generator with IEEE-488 Interface demonstrates how the MAX038 integrated circuit can be controlled using HP-VEE programming. The system can be used in an automated test environment to generate waveforms of various types at frequencies up to 15MHz.

The Waveform Generator with IEEE-488 interface also provides an excellent piece of test equipment for laboratory work.

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Title of Project

The Engineering Council Examination Part 2 (c)

Waveform Generator
With
IEEE Interface

Place Where Project was Undertaken

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Date of Submission of Project
28th May1999

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