A High Sensitivity CMOS Photoreceiver Incorporating a High Multiplication Gain Avalanche Photodiode

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Abstract — A Photoreceiver consisting of a monolithically integrated avalanche photodiode and a CMOS transimpedance amplifier is presented. The sensitivity has been analysed theoretically through simulations and a detailed noise analysis. Sensitivity results are presented based on the OEIC being fabricated in a 1.5 μm CMOS process. At 2 Gb/s the receiver has sensitivities of $-33.5 \text{ dBm}$ and $-34.7 \text{ dBm}$ for 650 nm and 850 nm light respectively, which exceed the performance of other reported CMOS photoreceivers.

Keywords — Avalanche photodiodes, optoelectronic integrated circuits (OEICs), photodetectors, photoreceivers.

I Introduction

The well known advantages of CMOS, namely high reliability, low cost and potential for large scale integration, together with the pressing need for short distance, short wavelength (≤ 850 nm) optical communications links, has meant there is currently an eagerness to produce a monolithically integrated CMOS photoreceiver. The difficulty with developing such a receiver is the monolithic integration of a high speed, high sensitivity photodiode with an amplifier, without adding complexity to the fabrication process.

Many CMOS monolithic photoreceivers have been developed to date [1, 2], however, reported receivers have shown a distinct trade-off between sensitivity and speed. On the other hand, standards for short wavelength interconnects, such as Fibre Channel and IEEE1394 (Firewire) require very high receiver sensitivities at high speed operation ($> -12.6 \text{ dBm}$ at $> 1 \text{ Gb/s}$ (Fibre Channel) and $> -21.0 \text{ dBm}$ at $> 100 \text{ Mb/s}$ (IEEE1394)) [3, 4]. This paper illustrates using simulations and noise analysis, that a CMOS photoreceiver incorporating a CMOS and SOI CMOS compatible Geiger-mode avalanche photodiode (GMAP) presents a possible solution to this trade-off. The simulations show that sensitivities of $> -25.0 \text{ dBm}$ can be obtained at 500 Mb/s when the photodiode is biased for multiplication gains in excess of 500 ($\approx 27.4 \text{ V reverse bias}$). The noise analysis shows that sensitivities of $> -40 \text{ dBm}$ are possible at 500 Mb/s and $> -30 \text{ dBm}$ achievable at 2 Gb/s.

II Photodiode

The photodetector used in the photoreceiver is a Geiger-mode avalanche photodiode. The GMAP, which is both CMOS and SOI CMOS compatible, has been designed for single photon counting [5]. A cross section of a GMAP is shown in Figure 1. The enrichment doping was tailored to provide the low (< 30 V) breakdown voltage. GMAPs of various dimensions have been fabricated. A small area GMAP with 20 μm active area diameter and 3 μm virtual guard ring overlap has been used here, due to its low capacitance (< 217 pF) and high bandwidth potential (2.75 GHz) [6, 7]. Characterisation of 20 μm active area GMAPs have also revealed high gain (1, 10, > 100 and > 1000 at 5.0 V, 27.0 V, 27.4 V and 27.5 V reverse bias respectively), high responsivity (0.05 A/W, 0.44 A/W, 15.21 A/W and 86.67 A/W at 5.0 V, 27.0 V, 27.4 V and 27.5 V reverse bias respectively) and low dark current (0.8 pA at 5 V reverse bias and 30 pA at 27.5 V reverse bias).

III Photoreceiver

The simulated CMOS photoreceiver [6, 8], incorporating the GMAP is shown in Figure 2. The simulations were made using Agilent Technologies’ microwave simulation software ADS (Advanced Design System). The MOSFETs were modelled using ADS Level 3 MOSFET models built us-
ing extracted SPICE Level 3 parameters for the NMRC (National Microelectronics Research Centre) 1.5 μm CMOS process. The GMAP was modelled using a capacitor and an AC current source. Although a GMAP has both junction capacitance and bondpad capacitance associated with it, only the junction capacitance is considered here, since bondpad capacitance is eliminated by the monolithic integration. The value of the junction capacitance was found from small signal equivalent circuit models for a 20 μm active area GMAP with 3 μm overlap [6, 7] built using measured $S_{11}$ parameters for the diode.

The photoreceiver is similar in design to those reported by A.V. Krishnamoorthy et al [9], and consists of a transimpedance amplifier ($M_1$, $M_2$, $M_{fn}$, $M_{fp}$) followed by a single inverter ($M_3$, $M_4$) that acts as a decision stage and generates logic levels. The transimpedance stage incorporates a CMOS inverter biased in the linear or gain region by the feedback resistance ($M_{fn}$, $M_{fp}$). Simulations of the inverter revealed gains of up to −19.2 are achievable (see Figure 3). Active feedback was used instead of the conventional passive feedback resistance because of its many advantages, including smaller size, full compatibility with OEIC fabrication processing and reduced parasitic feedback capacitance. The feedback consists of a diode connected NMOSFET in parallel with a PMOSFET. Simulations of the resistance have shown the resistance to vary from 22 kΩ to 39 kΩ, (depending on the input current (GMAP current)) and having an average value of 30.5 kΩ. Small signal AC simulations of the receiver for GMAP capacitances of 87.0 fF and 216.71 fF, corresponding to 27.5 V and 5 V reverse bias respectively, have been made and are shown in Figure 4. The simulations give an $f_{3dB}$ of 296 MHz and 132 MHz for 87.0 fF and 216.71 fF respectively, for an input current of 40 μA and $V_{cc} = 5.0$ V.

**IV Sensitivity**

A fundamental goal in the design of an optical receiver is to minimise the amount of optical power that must be received to achieve a given bit error rate (BER). This power, referred to as the sensitivity, depends upon the total noise of the photoreceiver front-end, the type of detector employed and the design of the amplifier. In this work, the
sensitivity of the photoreceiver is set by the threshold offset between the transimpedance amplifier inverter and the decision stage inverter ($\approx 0.5$ V). Basically, a large amount of photodiode current is needed to ensure that the output from the transimpedance amplifier causes the decision stage to switch. This current together with the GMAP responsivity sets the sensitivity.

The DC transfer characteristic at the output ($v_{out}$) of the photoreceiver has been simulated for various source voltages ($V_{cc}$) and is shown in Figure 5. The DC threshold currents (currents needed to switch the decision stage) can be clearly observed and increase with increasing $V_{cc}$. With $V_{cc} = 5.0$ V, 22.4 $\mu$A peak input current is needed for 3 V peak output voltage (or 0 – 3 V modulation), 27.2 $\mu$A is needed for 4 V, 43.2 $\mu$A is needed for 4.8 V and 68.8 $\mu$A for 4.9 V output. These currents have been used to compute the photoreceiver’s DC sensitivity for a range of GMAP multiplication gains (see Figure 6). Measurements of multiplication gain and responsivity versus reverse bias at 633 nm [6] were used in the computation. Clearly, very high sensitivities ($> -25$ dBm) are obtained for high multiplication gains ($> 500$), and Fibre Channel and IEEE1394 specifications are met for gains of $> 10$ and $> 70$ respectively.

Simulations have shown that as the frequency of operation of the photoreceiver increases, the required current increases and the sensitivity therefore decreases. Figure 7 shows the receiver sensitivity at 250 MHz (500 Mb/s) modulation. The minimum required peak current has increased to 27.5 $\mu$A, 32 $\mu$A, 50 $\mu$A and 70 $\mu$A for 3 V, 4 V, 4.8 V and 4.9 V peak output voltage respectively. Despite the increase in required current the sensitivity still remains high, due to the very high responsivity of the GMAP.

V Noise Limited Sensitivity

If a submicron CMOS process is used several additional gain stages can be added to the receiver, before the final decision stage. This leads to the elimination of the threshold offset between the two inverter stages. The photoreceiver sensitivity is then determined by the noise of the front–end and the type of detector incorporated. A detailed noise model of the photoreceiver has therefore been built and the receiver’s noise limited sensitivity analysed theoretically.

The noise model for the photoreceiver is shown in Figure 2. The model includes the following noise components:

- Shot noise due to the dark current $I_{dark}$ of the GMAP

$$\langle i_{PD}^2 \rangle = 2qI_{dark}I_2B.$$  \hspace{1cm} (1)

- Thermal noise due to the channel conductance
of the saturated MOSFETs $M_1$ and $M_2$

$$\langle i_m^2 \rangle = \frac{4kT}{g_{m1}} (2\pi CT)^2 I_3 B^3.$$  

$$\langle i_m^2 \rangle = \frac{4kT}{g_{m2}} (2\pi CT)^2 I_3 B^3.$$  

- Thermal noise due to the resistive channel of the saturated feedback MOSFET $M_{fn}$

$$\langle i_{f b}^2 \rangle = 4kT g_{mfn} I_2 B.$$  

- Thermal noise due to the resistive channel of the feedback MOSFET $M_{fp}$ operating in the linear region

$$\langle i_{f p}^2 \rangle = \frac{4kT}{r_{dsfp}} I_2 B.$$  

Where:

- $k$ = Boltzmann’s constant,
- $g_m$ = transconductance of the transistor,
- $r_{dsfp}$ = drain–source resistance of $M_{fp}$,
- $C_T$ = total input capacitance of the receiver,
- $T$ = temperature (Kelvin),
- $\Gamma$ = a material dependent numerical factor,
- $B$ = bitrate of the signal,
- $I_2$ = normalised noise bandwidth integral,
- $I_3$ = normalised noise bandwidth integral.

The total mean square noise input current is the sum of all the above contributions.

$$C_T = C_{PD} + C_{fb} + C_{in},$$  

$$C_{fb} = C_{gsfn} + C_{gsfp} + C_{dsfn} + C_{sbfp},$$  

$$C_{in} = C_{gs1} + C_{gs2} + (1 + A)(C_{gd1} + C_{gd2}),$$  

where:

- $C_{gs} =$ gate–source capacitance,
- $C_{gd} =$ gate–drain capacitance,
- $C_{sb} =$ source–bulk capacitance,
- $C_{db} =$ drain–bulk capacitance,
- $A =$ DC open loop gain of the amplifier.

The photodiode capacitance is the GMAP junction capacitance. The junction capacitance at various reverse bias voltages was again found from the equivalent circuit models [6, 7]. All the MOSFET capacitances were calculated using the SPICE Level 3 parameters for the 1.5 $\mu$m process and the formulae given in [10]. The DC open loop gain was obtained from simulations, and taken to be $-17.0$ ($V_{cc} = 5.0$ V) (see Figure 3). Again, it has been assumed that a 20 $\mu$m active area GMAP with 3 $\mu$m overlap has been used. The photodiode capacitance therefore varies from 216.71 fF to 87.14 fF (for reverse bias varying from 5 V to 27.5 V). $C_{fb}$ is calculated as being 16.97 fF and $C_{in}$ is found to be 36.99 fF. Noise calculations made for the photoreceiver assumed a rectangular NRZ signal, a synchronous optical link and a BER of $1 \times 10^{-12}$. This gives $I_2 = 0.56$ and $I_3 = 0.087$ [11]. The various noise currents have been calculated and the total mean input referred rms noise versus bandwidth is plotted in Figure 9 for a GMAP biased at 5 V and 27.5 V reverse bias. The dark current was obtained from measurements made on the GMAP [6] and $\Gamma$ was taken to be $2/3$ [10].

![Fig. 8: Small signal equivalent circuit of the open loop transimpedance preamplifier.](image)

![Fig. 9: Total mean input referred rms noise current, for GMAP biased at 5 V and 27.5 V reverse bias.](image)
where:  
\( \eta = \) photodiode external quantum efficiency, \( \overline{P} = \) average optical power incident on the detector, 
\( h = \) Planck’s constant, \( \nu = \) frequency of the incident light, \( q = \) electronic charge, \( Q = \) related to bit error probability, 
\( \langle i^2 \rangle_i = \) mean square noise current at receiver input, \( \langle M \rangle = \) mean avalanche gain, \( B = \) bitrate of the receiver, \( I_1 = \) normalised noise bandwidth integral, and \( F(\langle M \rangle) = \) excess noise factor due to the avalanche process.

For the conditions outlined above, and using Equation 9, the sensitivity has been calculated for various values of multiplication gain, a bitrate of 500 Mb/s and 650 nm and 850 nm light (see Figure 10). Measurements of gain versus voltage made on the GMAP [6] allowed for the determination of capacitance at various gains. Again, a NRZ signal, a synchronous optical link and a BER of \( 1 \times 10^{-12} \) were assumed, giving \( I_1 = 0.5 \) and \( Q = 7.04 \) [12].

It is clear from Figure 10 that there exists an optimum gain for which the sensitivity is highest, this optimum gain is given by Equation 10 [12].

\[
\langle M \rangle_{\text{opt}} = \frac{1}{k^{1/2}} \left( \frac{\langle i^2 \rangle_{\text{i}}^{1/2}}{\eta B I_1 Q} + k - 1 \right)^{1/2},
\]

(10)

where \( k = \) the ratio of ionisation coefficients of the holes and electrons in the detector junction. \( k \) has conservatively been taken to be 0.38 which is its value at breakdown [13]. The optimum gain has been calculated and has been found to be 25.28 for 650 nm and 850 nm light, and the corresponding sensitivities, at 500 Mb/s, are \(-41.11 \) dBm and \(-42.27 \) dBm respectively. Photoreceiver sensitivity versus bitrate has also been plotted and is shown in Figure 11. The sensitivity is very high and easily meets both Fibre Channel and IEEE1394 requirements. It is also worth noting that for a gain of 25, which corresponds to a photodiode reverse bias of 27.2 V, and at 2 Gb/s the sensitivity is \(-33.5 \) dBm and \(-34.7 \) dBm for 650 nm and 850 nm light respectively. These sensitivities are much higher than previous reports for CMOS monolithically integrated photoreceivers [1, 2]. The exceptional theoretical sensitivities obtained from the analysis, can of course be credited to both the very low photodiode capacitance and the internal gain of the GMAP. The sensitivity can be further improved through the use of a submicron CMOS process. A submicron process leads to a reduction in the total input capacitance \( C_T \) leading to reduced noise current and increased sensitivity.

A number of assumptions have been made in this analysis. Firstly, MOSFET gate leakage noise has been neglected, since gate leakage is so small its noise contribution is not significant. Secondly, it has been assumed that the component of the dark current that undergoes multiplication is small, including multiplied dark current requires a more rigorous analysis. Finally, the flicker noise or \( 1/f \) noise of the MOSFETs has been ignored, since very little is understood about MOSFET flicker noise and a consistent explanation of the noise generation has not yet emerged [10, 14]. However, it is known that flicker noise varies inversely with frequency and that it contributes substantially at lower frequencies (bitrates). Since the bitrates of interest here are relatively low (0–2 Gb/s), sensitivity calculations including flicker noise were also made to ensure that this noise source had no detrimental effect on sensitivity. The flicker noise of the MOSFETs was calculated using the equation used by Haralabidis et al [15] for the flicker noise of a MOSFET. The calculations showed that flicker noise had negligible effect on sensitivity at high multiplication gains (\( \geq 100 \)), as would be expected from Equation 9. The worst case, therefore, occurs for a multiplication gain of 1. At this gain
flicker noise reduces sensitivity by $\leq$ 2 dBm at low bitrates (10–500 Mb/s), and very little reduction at all occurs at higher bitrates (0.45 dBm and 0.24 dBm at 1 Gb/s and 2 Gb/s respectively).

VI Fabricated CMOS Photoreceiver
The CMOS photoreceiver was fabricated in a hybrid bulk/SOI CMOS process, where the GMAP was fabricated in the bulk handle wafer while the CMOS circuitry was implemented in the upper SOI layers. The photoreceiver was shown to operate to 10 MHz [16]. The initial measurement setup was poor and the GMAP had to be biased for very high multiplication gains ($\gg 100$), in order to get a response from the receiver. These high gains meant long multiplication buildup times which limited the bandwidth of the GMAP, and that of the photoreceiver, to the megahertz region. Sensitivity measurements were not made on the photoreceiver but will be made when an appropriate measurement setup is in place.

VII Conclusion
A CMOS monolithically integrated photoreceiver consisting of a GMAP biased in avalanche mode and a transimpedance amplifier has been presented. Sensitivity simulations together with a theoretical noise analysis have shown that the photoreceiver eliminates the trade-off between sensitivity and speed, usually observed in CMOS photoreceivers. Table 1 below shows a comparison between some of the highest performing CMOS photoreceivers reported and the receiver in this paper. Clearly, the reported photoreceivers have problems maintaining both high speed and high sensitivity. The highest sensitivity reported at 1 Gb/s is $-23.2$ dBm, while the highest reported at 2 Gb/s is a mere $-16.5$ dBm. The receiver reported here, however, has shown both high speed and high sensitivity operation ($> -25.0$ dBm at 500 Mb/s) through simulations, while the noise analysis has shown the potential for very high sensitivities at very high speed operation ($> -37.0$ dBm at 1 Gb/s and $> -33.0$ dBm at 2 Gb/s). To the best of the authors’ knowledge the achievable sensitivities reported here are higher than any sensitivities previously reported for CMOS photoreceivers.

VIII Acknowledgements
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References

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<th>Ref</th>
<th>Process (µm)</th>
<th>$V_{in}$ (V)</th>
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<td>0.13 CMOS on SOI</td>
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Table 1: Comparison of CMOS photoreceivers.


